Features

- **Qualified for Automotive Applications**
- **Wide Range of Digital and Analog Signal Levels**
  - **Digital: 3 V to 20 V**
  - **Analog: $\leq$ 20 $V_{P\text{-}P}$**
- **Low ON Resistance, 125 Ω (Typ) Over 15 $V_{P\text{-}P}$ Signal Input Range for $V_{DD} - V_{EE} = 18$ V**
- **High OFF Resistance, Channel Leakage of ± 100 pA (Typ) at $V_{DD} - V_{EE} = 18$ V**
- **Logic-Level Conversion for Digital Addressing Signals of 3 V to 20 V ($V_{DD} - V_{SS} = 3$ V to 20 V) to Switch Analog Signals to 20 $V_{P\text{-}P}$ ($V_{DD} - V_{EE} = 20$ V)**
- **Matched Switching Characteristics, $r_{on} = 5$ Ω (Typ) for $V_{DD} - V_{EE} = 15$ V**
- **Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2 μW (Typ) at $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10$ V**
- **Binary Address Decoding on Chip**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **100% Tested for Quiescent Current at 20 V**
- **Maximum Input Current of 1μA at 18 V Over Full Package Temperature Range, 100 nA at 18 V and 25$°$C**
- **Break-Before-Make Switching Eliminates Channel Overlap**

Applications

- **Analog and Digital Multiplexing and Demultiplexing**
- **Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Conversion**
- **Signal Gating**

description/ordering information

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches that have low ON impedance and very low OFF leakage current. Control of analog signals up to 20 $V_{P\text{-}P}$ can be achieved by digital signal amplitudes of 4.5 V to 20 V (If $V_{DD} - V_{SS} = 3$ V, a $V_{DD} - V_{EE}$ of up to 13 V can be controlled; for $V_{DD} - V_{EE}$ level differences above 13 V, a $V_{DD} - V_{SS}$ of at least 4.5 V is required). For example, if $V_{DD} = 4.5$ V, $V_{SS} = 0$ V, and $V_{EE} = -13.5$ V, analog signals from –13.5 V to 4.5 V can be controlled by digital inputs of 0 V to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic high (H) is present at the inhibit (INH) input, all channels are off.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC – M	Reel of 2500	CD4051BQM96Q1	CD4051Q
	TSSOP – PW	Reel of 2000	CD4051BQPWRQ1	CM051BQ
	SOIC – M	Reel of 2500	CD4052BQM96Q1§	CD4052Q
	TSSOP – PW	Reel of 2000	CD4052BQPWRQ1§	CD4052Q
	SOIC – M	Reel of 2500	CD4053BQM96Q1	CD4053Q
	TSSOP – PW	Reel of 2000	CD4053BQPWRQ1§	CD4053Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Product Preview

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

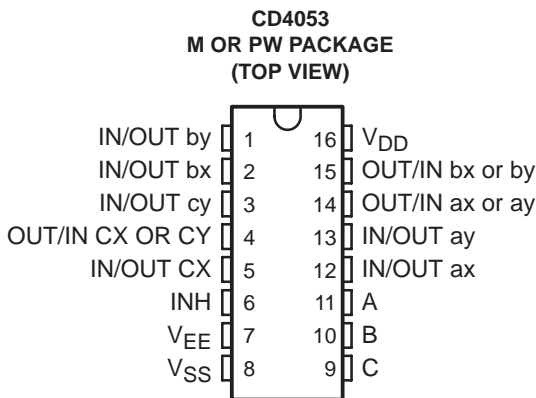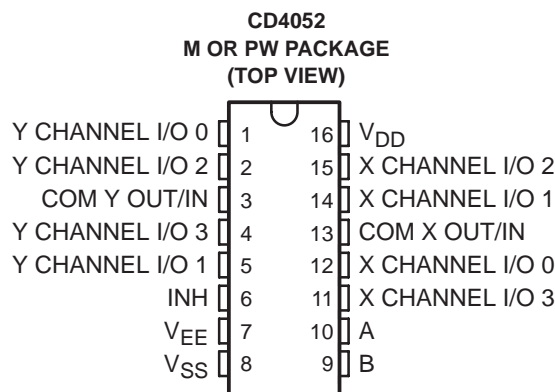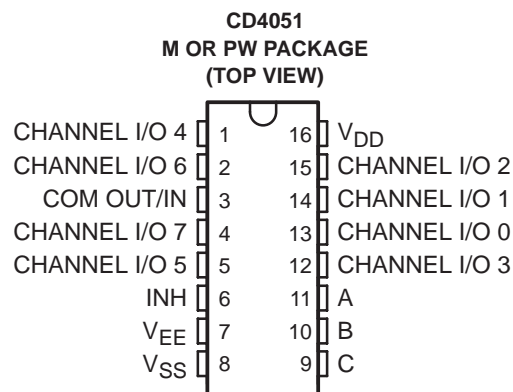Copyright © 2008, Texas Instruments Incorporated

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description/ordering information (continued)

The CD4051B is a single eight-channel multiplexer that has three binary control inputs (A, B, and C) and an inhibit input. The three binary signals select one of eight channels to be turned on and connect one of the eight inputs to the output.

The CD4052B is a differential four-channel multiplexer that has two binary control inputs (A and B) and an inhibit input. The two binary input signals select one of four pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple two-channel multiplexer with three separate digital control inputs (A, B, and C) and an inhibit input. Each control input selects one of a pair of channels, which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs, and the common (COM OUT/IN) terminals are the inputs.

CD4051
M OR PW PACKAGE
(TOP VIEW)

CHANNEL I/O 4	1		16	V_{DD}
CHANNEL I/O 6	2		15	CHANNEL I/O 2
COM OUT/IN	3		14	CHANNEL I/O 1
CHANNEL I/O 7	4		13	CHANNEL I/O 0
CHANNEL I/O 5	5		12	CHANNEL I/O 3
INH	6		11	A
V_{EE}	7		10	B
V_{SS}	8		9	C

CD4052
M OR PW PACKAGE
(TOP VIEW)

Y CHANNEL I/O 0	1		16	V_{DD}
Y CHANNEL I/O 2	2		15	X CHANNEL I/O 2
COM Y OUT/IN	3		14	X CHANNEL I/O 1
Y CHANNEL I/O 3	4		13	COM X OUT/IN
Y CHANNEL I/O 1	5		12	X CHANNEL I/O 0
INH	6		11	X CHANNEL I/O 3
V_{EE}	7		10	A
V_{SS}	8		9	B

CD4053
M OR PW PACKAGE
(TOP VIEW)

IN/OUT by	1		16	V_{DD}
IN/OUT bx	2		15	OUT/IN bx or by
IN/OUT cy	3		14	OUT/IN ax or ay
OUT/IN CX OR CY	4		13	IN/OUT ay
IN/OUT CX	5		12	IN/OUT ax
INH	6		11	A
V_{EE}	7		10	B
V_{SS}	8		9	C

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Function Tables

CD4051

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	None

X = don't care

CD4052

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	0x, 0y
L	L	H	1x, 2y
L	H	L	2x, 2y
L	H	H	3x, 3y
H	X	X	None

X = don't care

CD4053

INPUTS		ON CHANNEL
INH	A OR B OR C	
L	L	ax or bx or cx
L	H	ay or by or cy
H	X	None

X = don't care

logic diagram (positive logic)
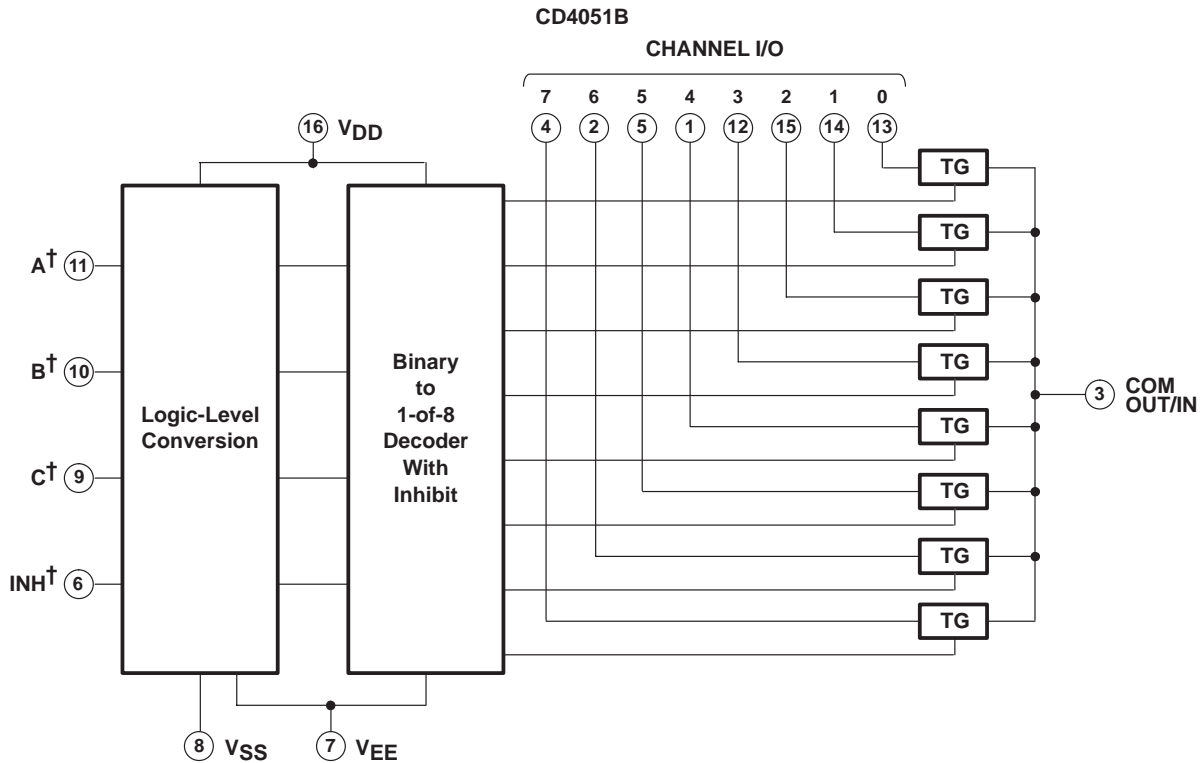
† All inputs are protected by CMOS protection network.
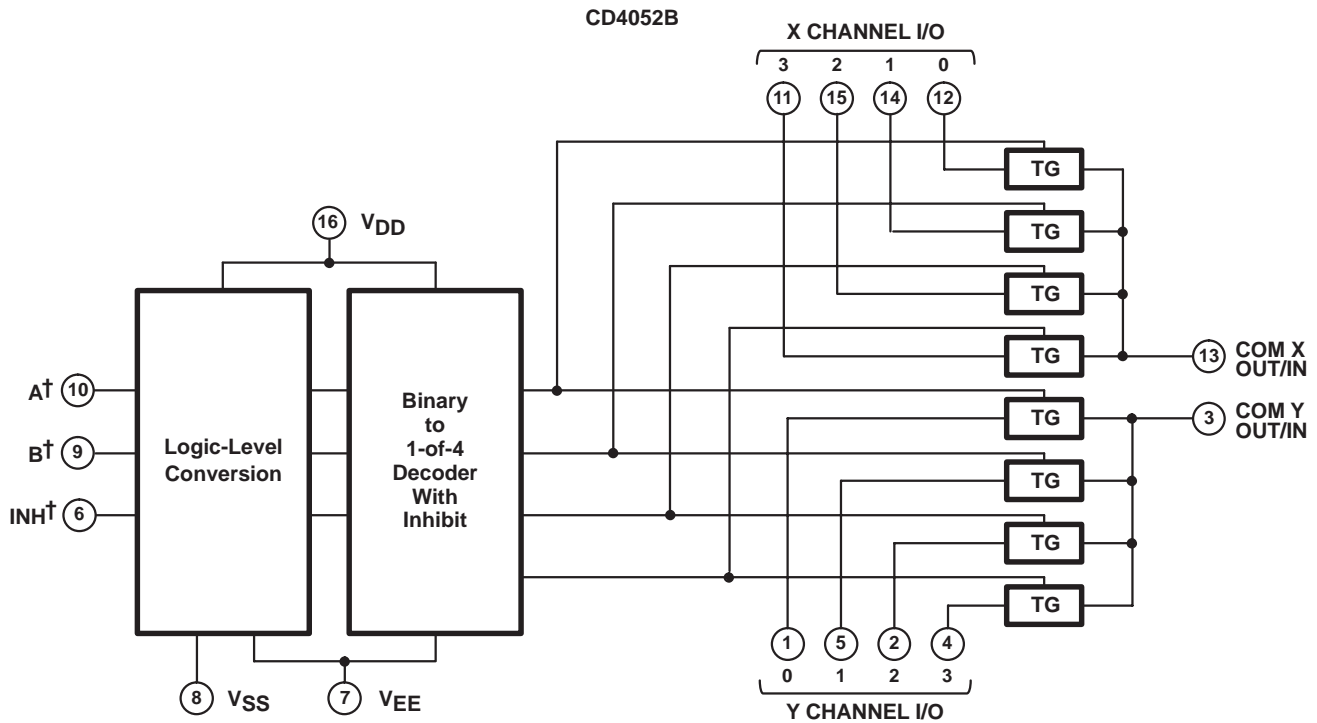
† All inputs are protected by CMOS protection network.

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logic diagrams (positive logic) (continued)

CD4053B
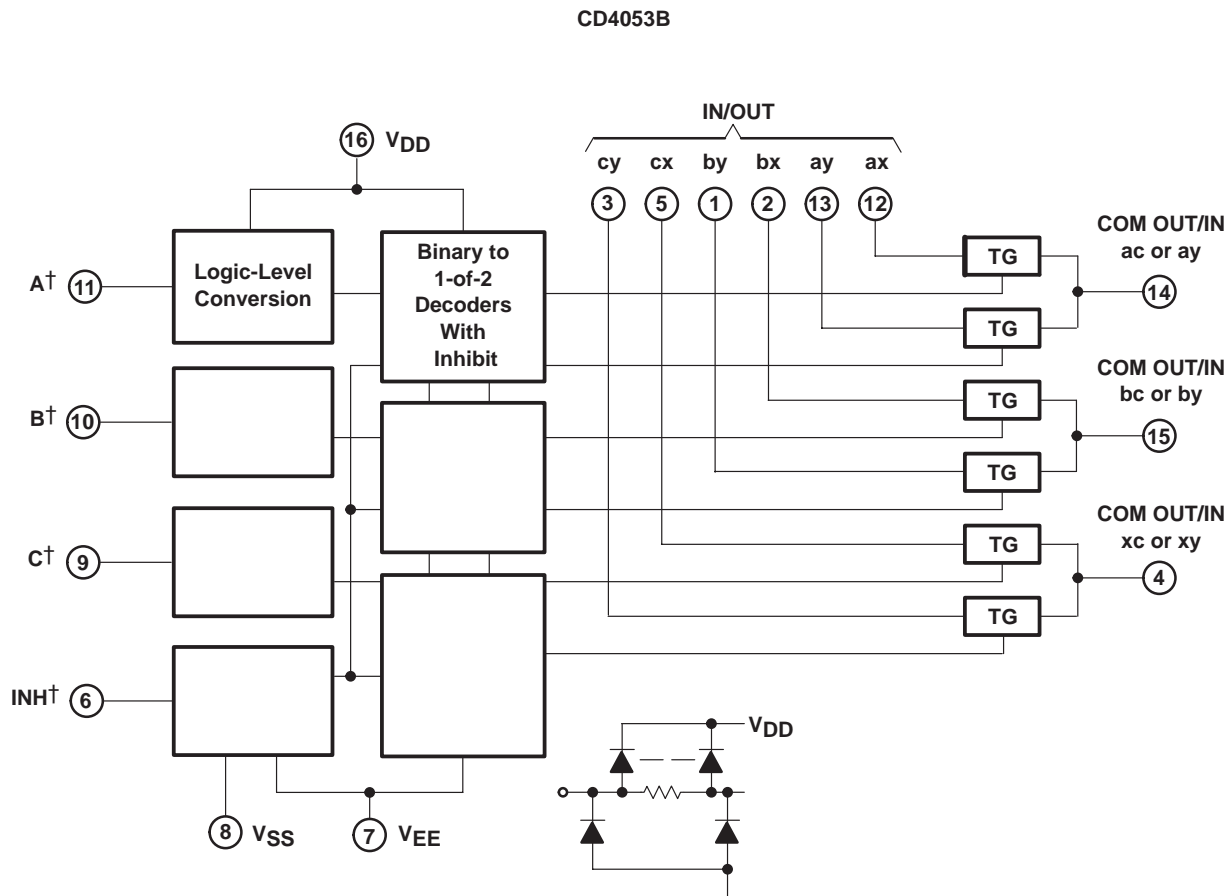
† All inputs are protected by standard CMOS protection network.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage range, V+ to V− (voltages referenced to V_{SS} terminal) .... −0.5 to 20 V

DC input voltage range .... −0.5 V to V_{DD} + 0.5 V

DC input current, any one input .... ±10 mA

Package thermal impedance, θ_{JA} (see Note 1): M package .... 73°C/W

PW package .... 108°C/W

Maximum junction temperature, T_J .... 150°C

Lead temperature (during soldering):

At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max .... 265°C

Storage temperature range, T_{stg} .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	5	20	V
T_A	Operating free-air temperature	−40	125	°C

electrical characteristics, $V_{SUPPLY} = \pm5$ V, $A_V = 1$ V, $R_L = 100\ \Omega$, unless otherwise noted (see Note 2)

PARAMETER		TEST CONDITIONS		V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES					UNIT
					−40°C	125°C	25°C			
							MIN	TYP	MAX	
I_{DD}	Quiescent device current			5	5	150		0.04	5	μA
				10	10	300		0.04	10	
				15	20	600		0.04	20	
				20	100	3000		0.08	100	
Signal Input (V_{is}) and Output (V_{os})										
r_{on}	Drain-to-source ON-state resistance	$V_{EE} = 0$ V, $V_{SS} = 0$ V, $V_{IS} = 0$ to V_{DD}		5	850	1300		470	1050	Ω
				10	330	550		180	400	
				15	210	320		125	240	
Δr_{on}	ON-state resistance difference between any two switches	$V_{EE} = 0$ V, $V_{SS} = 0$ V		5				15		Ω
				10				10		
				15				5		
	Input/output leakage current (switch off)	Any channel OFF (MAX) or all channels OFF (COM OUT/IN) (Max), $V_{EE} = 0$ V, $V_{SS} = 0$ V, See Note 3		18	±0.1	±1		$\pm10^{-5}$	±0.1	μA
C_{is}	Input capacitance	$V_{EE} = -5$ V, $V_{SS} = -5$ V		5				5		pF
C_{os}	Output capacitance	$V_{EE} = -5$ V, $V_{SS} = -5$ V	CD4051	5				30		pF
			CD4052					18		
			CD4053					9		
C_{ios}	Feedthrough capacitance	$V_{EE} = -5$ V, $V_{SS} = -5$ V		5				0.2		pF
t_{pd}	Propagation delay (signal input to output)	$V_{IS(p-p)} = V_{DD}$, $R_L = 200$ kΩ, $C_L = 50$ pF, t_r, $t_f = 20$ ns		5				30	60	ns
				10				15	30	
				15				10	20	

NOTES: 2. Peak-to-peak voltage symmetrical about $\dfrac{V_{DD} - V_{EE}}{2}$

3. Determined by minimum feasible leakage measurement for automatic testing

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electrical characteristics, V_{SUPPLY} = ±5 V, A_V = 1 V, R_L = 100 Ω, unless otherwise noted (see Note 2) (continued)

PARAMETER		TEST CONDITIONS	V_{EE} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES					UNIT
					–40°C	125°C	25°C			
							MIN	TYP	MAX	
Control (Address or Inhibit), V_C										
V_{IL}	Input low voltage	V_{IL} = V_{DD} through 1kΩ, V_{IH} = V_{DD} through 1kΩ, R_L = 1kΩ to V_{SS}, I_{is} < 2 µA on all OFF channels	V_{SS}	5	1.5	1.5			1.5	V
			V_{SS}	10	3	3			3	
			V_{SS}	15	4	4			4	
V_{IH}	Input high voltage	V_{IL} = V_{DD} through 1kΩ, V_{IH} = V_{DD} through 1kΩ, R_L = 1kΩ to V_{SS}, I_{is} < 2 µA on all OFF channels	V_{SS}	5	3.5	3.5	3.5			V
			V_{SS}	10	7	7	7			
			V_{SS}	15	11	11	11			
I_{IN}	Input current	V_{IN} = 0 V, 18 V		18	±0.1	±1	±10[3]		±0.1	µA
t_{pd1}	Address-to-signal OUT (channels ON or OFF) propagation delay	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ, V_{SS} = 0 V, See Figure 10, Figure 11, and Figure 14	0	5				450	720	ns
			0	10				160	320	
			0	15				120	240	
			–5	5				225	450	
t_{pd2}	Inhibit-to-signal OUT (channel turning ON) propagation delay	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ, V_{SS} = 0 V, See Figure 11	0	5				400	720	ns
			0	10				160	320	
			0	15				120	240	
			–10	5				200	400	
t_{pd3}	Inhibit-to-signal OUT (channel turning OFF) propagation delay	t_r, t_f = 20 ns, C_L = 50 pF, R_L = 10 kΩ, V_{SS} = 0 V, See Figure 15	0	5				200	450	ns
			0	10				90	210	
			0	15				70	160	
			–10	5				130	300	
C_{IN}	Input capacitance, any address or inhibit input							5	7.5	pF

NOTES: 2: Peak-to-peak voltage symmetrical about $\dfrac{V_{DD} - V_{EE}}{2}$

3: Determined by minimum feasible leakage measurement for automatic testing

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electrical specifications

PARAMETER		TEST CONDITIONS		V_{IS} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES 25°C			UNIT
						MIN	TYP	MAX	
	−3-dB cutoff frequency, channel ON (sine-wave input)	$R_L = 1$ kΩ, V_{OS} at COM OUT/IN, See Note 2, V_{OS} at COM OUT/IN	CD4053	5	10		30		MHz
			CD4052	5	10		25		
			CD4051	5	10		20		
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -3$ dB, V_{OS} at any channel					60		
THD	Total harmonic distortion	$R_L = 10$ kΩ, See Note 2		2	5		0.3		%
				3	10		0.2		
				5	15		0.12		
		$V_{EE} = V_{SS}$, $f_{is} = 1$-kHz sine wave					0.12		
	−40-dB feedthrough frequency (all channels OFF)	$R_L = 1$ kΩ, V_{OS} at COM OUT/IN, See Note 2	CD4053	5	10		8		MHz
			CD4052	5	10		10		
			CD4051	5	10		12		
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -40$ dB, V_{OS} at any channel					8		
	−40-dB signal crosstalk frequency	$R_L = 1$ kΩ, between any two channels, See Note 2		5	10		3		MHz
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -40$ dB, Between sections, Measured on common	CD4052				6		
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -40$ dB, Between sections, Measured on any channel					10		
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -40$ dB, Between any two sections, In pin 2, Out pin 14	CD4053				2.5		
		$V_{EE} = V_{SS}$, 20log $V_{OS}/V_{IS} = -40$ dB, Between any two sections, In pin 15, Out pin 14					6		
	Address or inhibit to signal crosstalk	$R_L = 10$ kΩ, See Note 4			10		65		mV$_{PEAK}$
		$V_{EE} = 0$ V, $V_{SS} = 0$ V, t_r, $t_f = 20$ ns, $V_{CC} = V_{DD} - V_{SS}$ (square wave)					65		

NOTES: 2. Peak-to-peak voltage symmetrical about $\dfrac{V_{DD} - V_{EE}}{2}$

4. Both ends of channel

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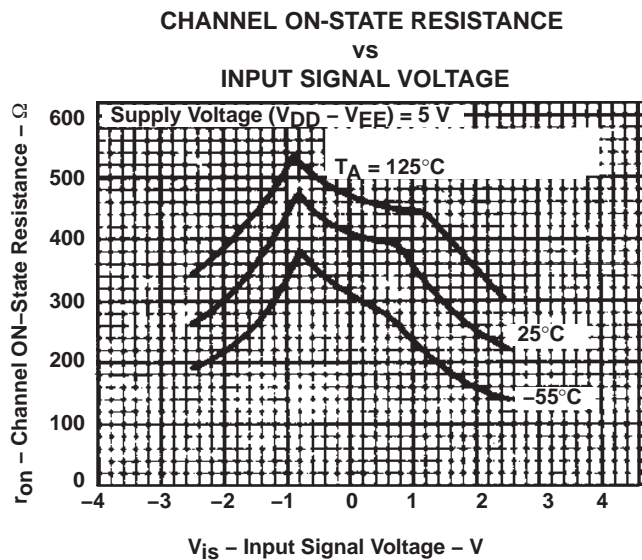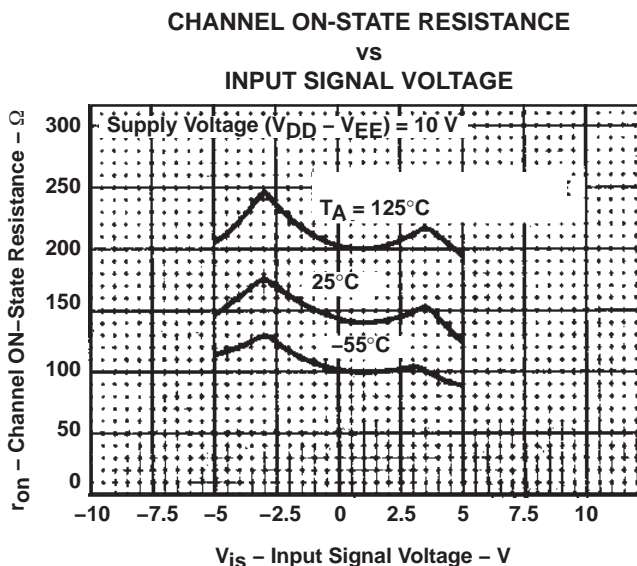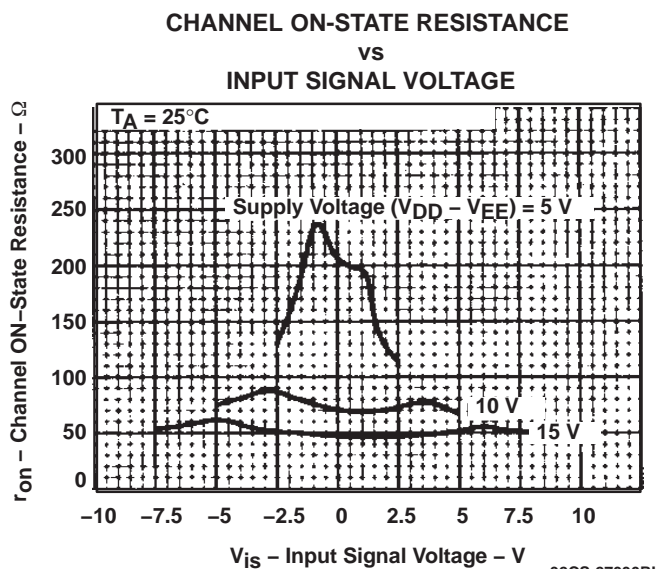
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TYPICAL CHARACTERISTICS

CHANNEL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE

Figure 1

CHANNEL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE

Figure 2

CHANNEL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE

Figure 3

CHANNEL ON-STATE RESISTANCE
vs
INPUT SIGNAL VOLTAGE

Figure 4

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9
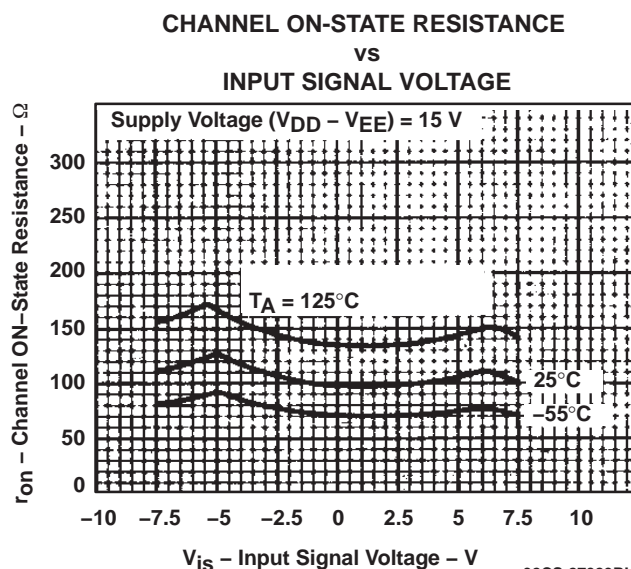
TYPICAL CHARACTERISTICS

**ON CHARACTERISTICS FOR
1-OF-8 CHANNELS (CD4051B)**
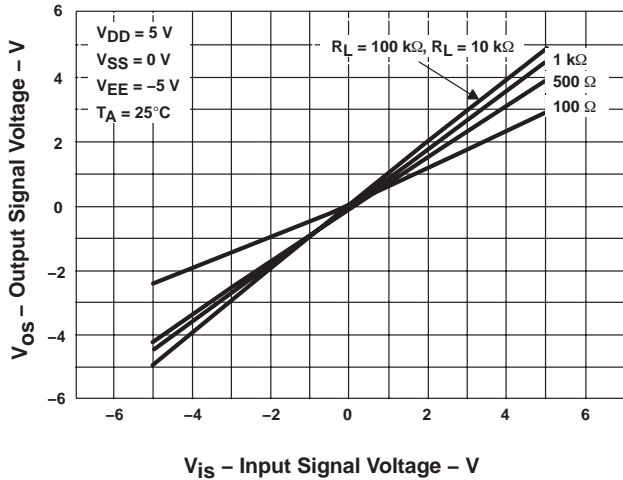
Figure 5

**DYNAMIC POWER DISSIPATION
vs
SWITCHING FREQUENCY (CD4051B)**
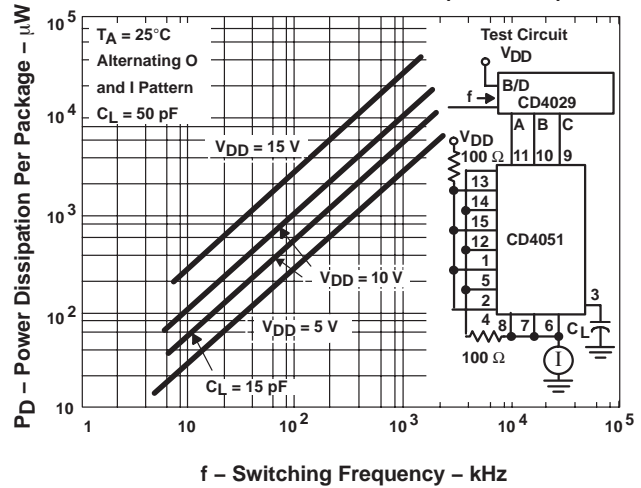
Figure 6

**DYNAMIC POWER DISSIPATION
vs
SWITCHING FREQUENCY (CD4052B)**
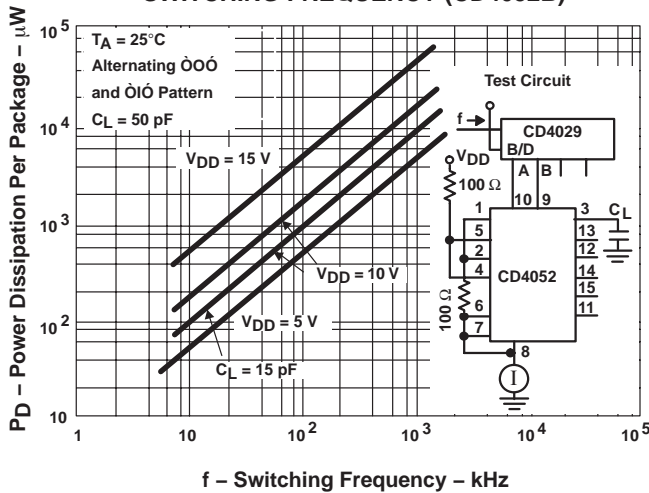
Figure 7

**DYNAMIC POWER DISSIPATION
vs
SWITCHING FREQUENCY (CD4053B)**
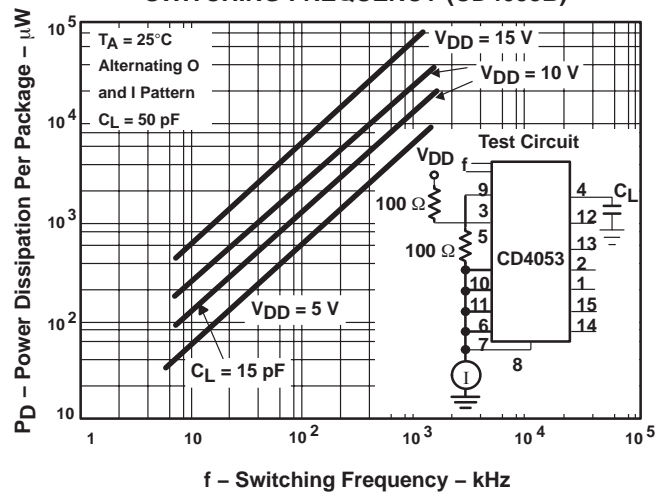
Figure 8

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PARAMETER MEASUREMENT INFORMATION
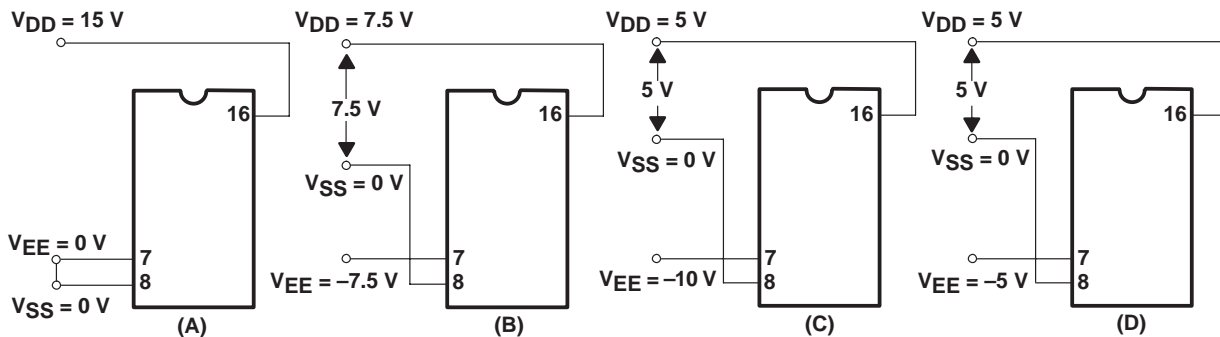
NOTE: The A, B, C, and INH input logic levels are L = V_{SS} and H = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Figure 9. Typical Bias-Voltage Test Circuits
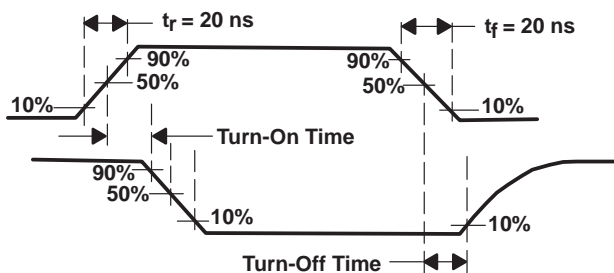
Figure 10. Channel Turned ON Waveforms
(R_L = 1 kΩ)
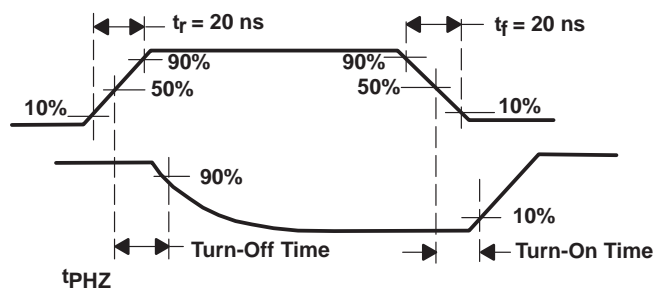
Figure 11. Channel Turned OFF Waveforms
(R_L = 1 kΩ)

PARAMETER MEASUREMENT INFORMATION
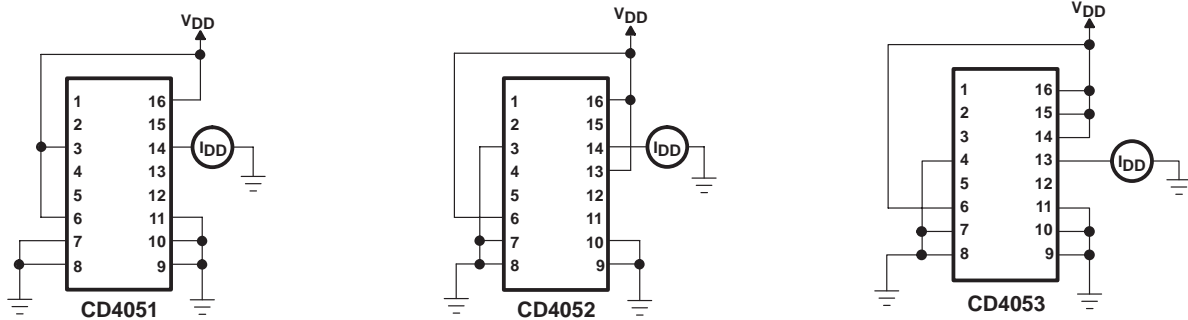
Figure 12. OFF Channel Leakage Current, Any Channel OFF
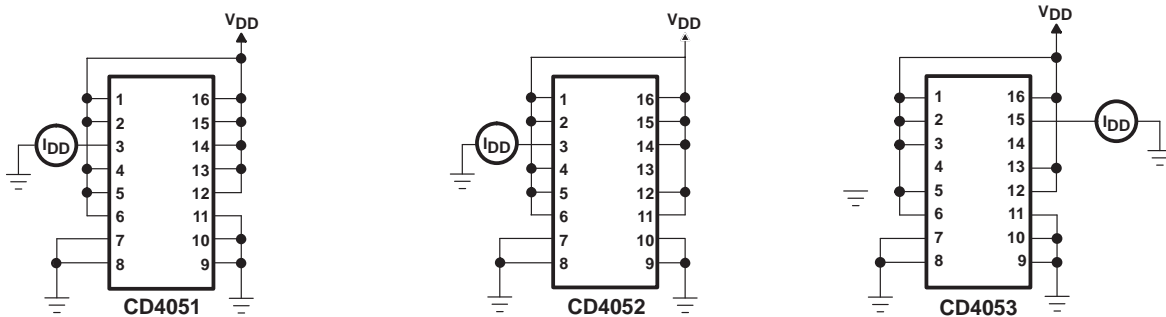
Figure 13. OFF Channel Leakage Current, All Channels OFF
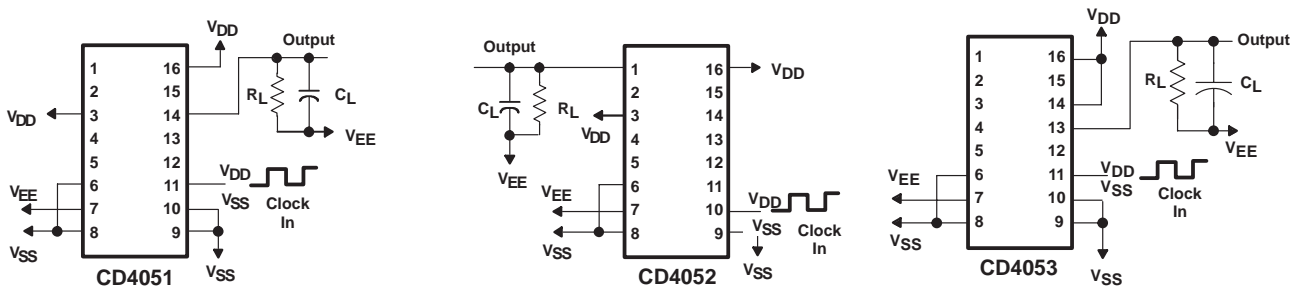
Figure 14. Propagation Delay, Address Input to Signal Output
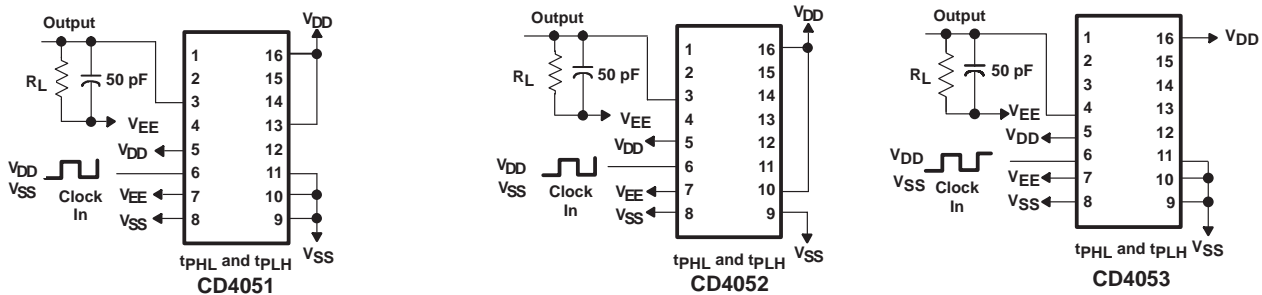
Figure 15. Propagation Delay, Inhibit Input to Signal Output

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PARAMETER MEASUREMENT INFORMATION
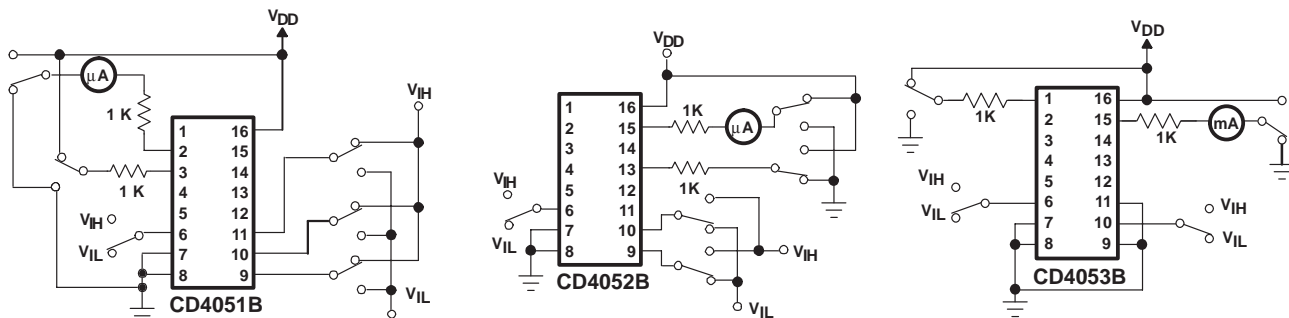
Measure <2 μA on All OFF Channels (e.g., Channel 6)

Measure <2 μA on All OFF Channels (e.g., Channel 2x)

Measure <2 μA on All OFF Channels (e.g., Channel by)

Figure 16. Input-Voltage Test Circuit (Noise Immunity)
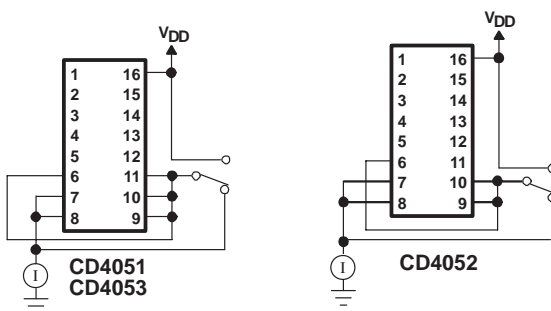
Figure 17. Quiescent Device Current
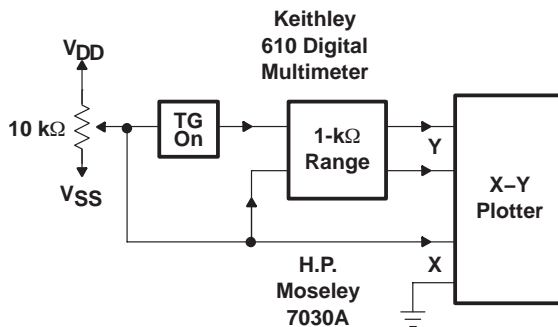
Figure 18. Channel ON-Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION
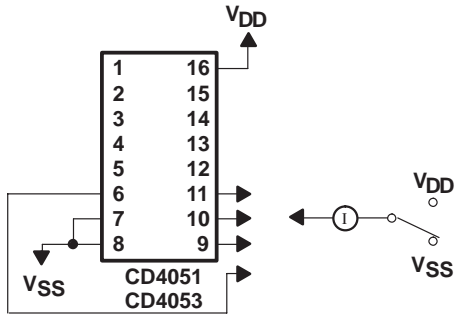
NOTE: Measure inputs sequentially to both V_{DD} and V_{SS}.
Connect all unused inputs to either V_{DD} or V_{SS}.
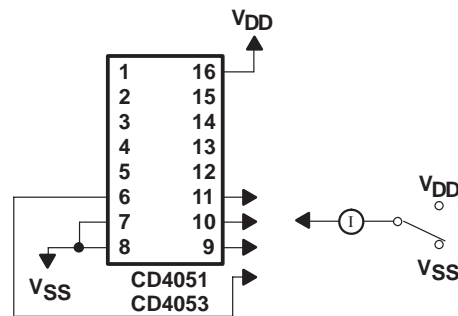
NOTE: Measure inputs sequentially to both V_{DD} and V_{SS}.
Connect all unused inputs to either V_{DD} or V_{SS}.

Figure 19. Input Current
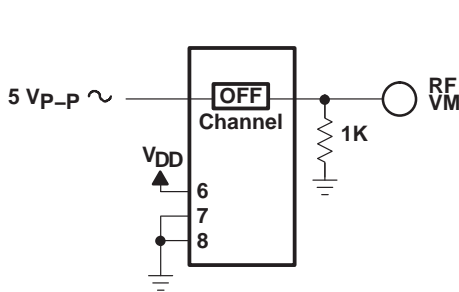
Figure 20. Feedthrough
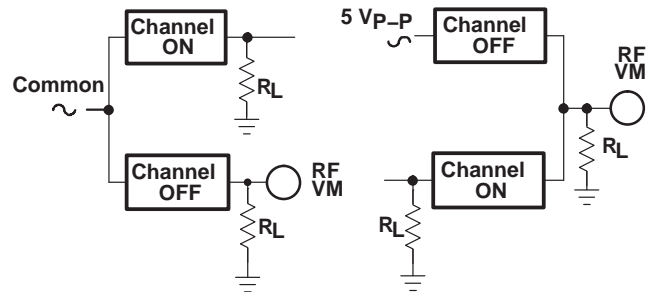
Figure 21. Crosstalk Between Any Two Channels
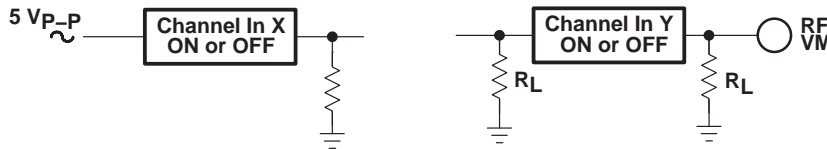
Figure 22. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)
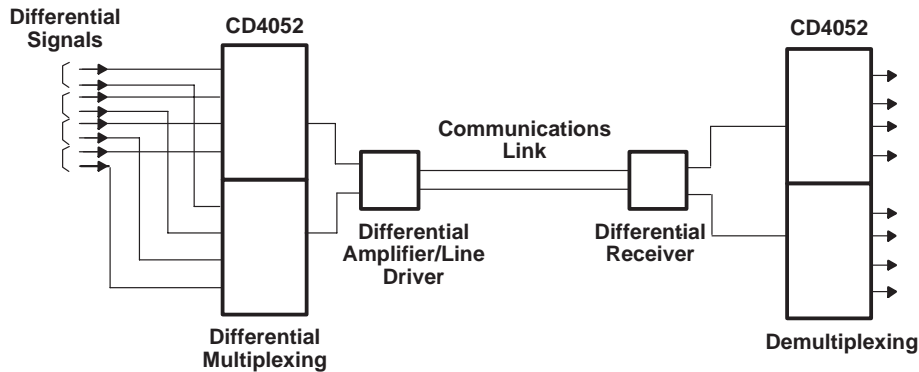
Figure 23. Typical Time-Division Application of the CD4052B

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APPLICATION INFORMATION

In applications where separate power sources drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.
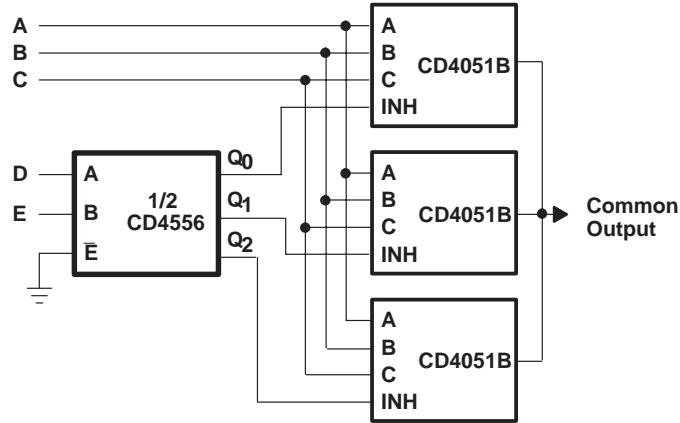
Figure 24. 24-to-1 Multiplexer Addressing

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4051BQPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4053BQM96Q1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R−PDSO−G16)   **PLASTIC SMALL−OUTLINE PACKAGE**

0.394 (10,00)
0.386 (9,80)

⟨C⟩

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/H 11/2006
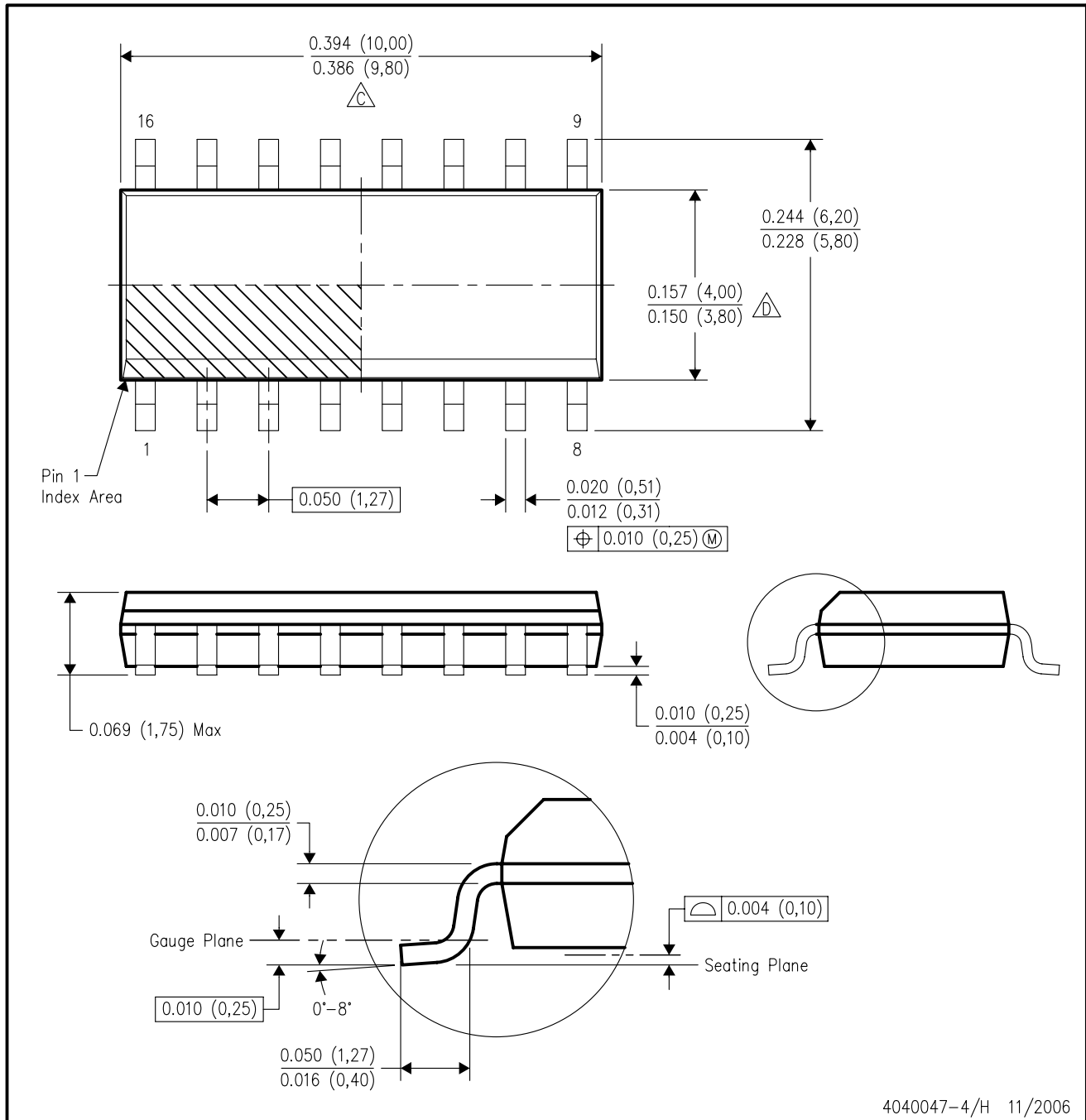
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
       ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
       ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AC.

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE